REMARKS

This is a full and timely response to the outstanding Action mailed February 17, 2005. Upon entry of the amendments in this response, claims 1-5, 7-13, 15-19 and 21-27 remain pending. In particular, Applicants have amended claims 1, 9, 15 and 13 and cancelled claims 4, 12, 18 and 26 without waiver, disclaimer or prejudice. Applicants have cancelled claims 4, 12, 18 and 26 merely to reduce the number of disputed issues and to facilitate early allowance and issuance of the remaining claims in the present application. Additionally, claims 1, 9, 15 and 13 are amended herein to further recite the limitations of "a fourth lightly doped region of the second type adjacent to the first doped region and beneath the gate", "an N lightly doped region adjacent to the first N+ doped region in the first P well and beneath the first gate and a P lightly doped region adjacent to the second P+ doped region in the second N well and beneath the second gate", "forming a fourth lightly doped region of the second type adjacent to the first doped region and beneath the gate" and "forming a N lightly doped region adjacent to the first N+ doped region in the first P well and beneath the first gate and forming a P lightly doped region adjacent to the second P+ doped region in the second N well and beneath the second gate", respectively. These features are shown in Figs. 4 and 5 of the application, wherein a N lightly doped region 433 is adjacent to the first N+ doped region 431 in the first P well 411 and beneath the first gate 420and a P lightly doped region 533 is adjacent to the second P+ doped region 531 in the second N well 511 and beneath the second gate 520. Accordingly, no new matter has been added. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Objection to the Specification and Rejections under 35 U.S.C 112

The Office Action objected to the specification under 37 CFR 1.75(d)(1) and MPEP § 608.01(o) as allegedly failing to provide proper antecedent basis for the claimed subject matter. The Office Action further rejected claims 1-5, 7-13, 15-19 and 21-27 under 35 USC 112, first paragraph, as allegedly failing to comply with the written description requirement. As set forth herein, Applicants respectfully traverse these objections and rejections.

The Office Action indicated that, although FIGs. 4 and 5 appear to disclose no field oxide between a gate and first and second wells, these drawings are merely isolated cross-sections that do not fully represent the device. Moreover, the Office Action alleged that in reality both the gate and the well regions extend into and out of the page, thus it is possible to have a field oxide between the gate and the well regions at another location in the device not shown by the figures.

With respect to FIG. 5 of the cited reference (US 6,307,224), FIG. 5 shows a perspective side view of a semiconductor device. In FIG. 5, there is not a field oxide between the gate 26 and the well regions 22 and 27 at another location in the active region of the device (i.e. any location where both the gate 26 and the well regions 22 and 27 extend into and out of the page showing FIG. 4A). Now turning to FIGs, 4 and 5 of the present application, note that FIGs, 4 and 5 are cross-sections showing a transistor in an active region defined by the field oxides 450. In the active region, however, such merely isolated cross-sections can fully represent the device. The Examiner is reminded that a single high-voltage device (transistor) should be located in the active region. That is, it is impossible to have a field oxide between the gate and the well regions at another location in the active region of the device not shown by the figures. Additionally, Applicants respectfully assert that the objection to the specification and the rejections as to these claims have been rendered moot.

Rejections under 35 U.S.C. 102 and 103

The Office Action rejected claims 1, 5, 15 and 19 under 35 U.S.C 102(b) as allegedly anticipated by *Shirai* (US Pat. 6,307,224). The Office Action further rejected claims 2 and 16 under 35 U.S.C 103(a) as allegedly unpatentable over *Shirai* in view of *Ito et al.* (US Pat. 5,856,695). Moreover, the Office Action rejected claims 3, 4, 17 and 18 under 35 U.S.C 103(a) as allegedly unpatentable over *Shirai* in view of *McElheny et al.* (US Pat. 6,740,944) and claims 7 and 21 were rejected under 35 U.S.C 103(a) as allegedly unpatentable over *Shirai*. Additionally, the Office Action rejected claims 8 and 22 under 35 U.S.C 103(a) as allegedly unpatentable over *Shirai* in view of *Liu et al.* (US Pat. 6,265,752). Applicant respectfully traverses the rejections for at least the reasons set forth herein.

With respect to *Shirai*, *Shirai* discloses a double diffused MOSFET consists of a p-type impurity diffusion region 14 formed on the semiconductor layer 11, an n^+ -type source region 16 formed in a surface area in the p-type impurity diffusion region 14, a gate insulating layer 17 formed on the p-type impurity diffusion region 14 and covering a region between the source region and the semiconductor layer 11, a gate electrode 18 formed on the gate insulating layer 17, an n^+ -type drain region 21 formed on the semiconductor layer 11 at a predetermined position separated from the p-type impurity diffusion region 14, and an n-type well 19 formed around the drain region (see the abstract and FIG. 3A). Note that *Shirai* does not disclose or teach a lightly doped region adjacent to the source region 16 and beneath the gate 18.

In this regard, the Office Action indicates the difference between *Shirai* and the claimed invention is a fourth lightly doped region of the second type adjacent to the first doped conducting layer and beneath one of the spacers. However, FIG. 1B of *McElheny* discloses a MOSFET with sidewall spacers and light doped regions beneath the spacers (LDD structure).

The ordinary artisan would have been motivated to modify *Shirai* in the manner described above for the purpose of further isolating the gate to prevent build-up of device capacitance and further suppressing hot carrier generation. Applicants respectfully disagree. Note that n^+ -type source region 16 disclosed by *Shirai* is laterally extended beneath the gate electrode 18 and the gate insulating layer 17. There is no reason to additionally form a light doped region beneath the gate 18 and it is very difficult to form an additional light doped region in the device disclosed by *Shirai* due to extension of the n^+ -type source region 16. Moreover, the device shown in FIG. 1B of *McElheny* is a MOSFET with a general MOS structure, rather than a high voltage device structure. Although the MOSFET shown in FIG. 1B of *McElheny* includes a lightly doped region 40, there is no suggestion or evidence that the lightly doped region 40 disclosed by *McElheny* can appropriately apply to the high voltage device of *Shirai* . Therefore, Applicant respectfully asserts that there is no motivation to combine *Shirai* and *McElheny* .

Turning now to the amended claims, claim 1 recites:

> 1. A high voltage device comprising:
>
> a substrate;
>
> first and second wells respectively of a first type and a second type in the substrate;
>
> a gate formed on a junction between the first and second wells, without a field oxide between the gate and the first and second wells;
>
> first and second doped regions both of the second type, respectively formed in the first and second wells and both sides of the gate;
>
> a third doped region of the first type in the first well and adjacent to the first doped region; and
>
> ***a fourth lightly doped region of the second type adjacent to the first doped region and beneath the gate.***

(*Emphasis Added*).

Additionally, claim 9 recites:

> 9. A high voltage device formed on a P substrate comprising:
> an HVNMOS comprising:

first P and N wells in the P substrate;

a first gate formed on a junction between the first P and N wells, without a field oxide between the gate and the first P and N wells;

two first N+ doped regions respectively formed in the first P and N wells, and both sides of the first gate;

a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and

an N lightly doped region adjacent to the first N+ doped region in the first P well and beneath the first gate; and

a HVPMOS comprising:

an N+ buried layer in the P substrate;

second N and P wells in the P substrate and above the N+ buried layer;

a second gate formed on a junction between the second N and P wells, without a field oxide between the gate and the second P and N wells;

two second P+ doped regions respectively formed in the second N and P wells, and both sides of the second gate;

a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well; and

a P lightly doped region adjacent to the second P+ doped region in the second N well and beneath the second gate.

(*Emphasis Added*).

Additionally, claim 15 recites:

15. A method for manufacturing a high voltage device, comprising the steps of:

providing a substrate;

forming first and second wells respectively of a first type and a second type in the substrate;

forming a gate on a junction between the first and second wells, without a field oxide formed between the gate and the first and second wells;

forming first and second doped regions both of the second type, respectively in the first and second wells and both sides of the gate;

forming a third doped region of the first type in the first well and adjacent to the first doped region; and

forming a fourth lightly doped region of the second type adjacent to the first doped region and beneath the gate.

(*Emphasis Added*).

Further, claim 23 recites:

23. A method for manufacturing a high voltage device comprising the steps of:

providing a P substrate;
forming a HVNMOS on the P substrate by:
forming first P and N wells in the P substrate;
forming a first gate on a junction between the first P and N wells, without a field oxide between the gate and the first P and N wells;
forming two first N+ doped regions respectively in the first P and N wells, and both sides of the first gate;
forming a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and
forming a N lightly doped region adjacent to the first N+ doped region in the first P well and beneath the first gate; and
forming a HVPMOS on the P substrate by:
forming an N+ buried layer in the P substrate;
forming second N and P wells in the P substrate and above the N+ buried layer;
forming a second gate on a junction between the second N and P wells, without a field oxide between the gate and the second P and N wells;
forming two second P+ doped regions respectively in the second N and P wells, and both sides of the second gate;
forming a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well; and
forming a P lightly doped region adjacent to the second P+ doped region in the second N well and beneath the second gate.

(*Emphasis Added*). Applicants submit that the foregoing independent claims patently define over the cited art of record for at least the reason that the cited art fails to disclose the features emphasized (bold and italics) above.

According to MPEP 2143, to establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Applicants respectfully submit that, even combined, *Shirai* and *McElheny* fail to teach at least the elements emphasized in the independent claims above. In addition Applicants respectfully assert that *Shirai* and *McElheny* do not teach or reasonably suggest at least the features/limitations that have been emphasized above in independent claims 1, 9, 15 or 23, nor is there a proper motivation to combine the selected features *Shirai* with *McElheny*. Consequently,

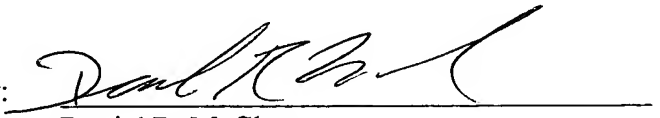
Applicants respectfully assert that the rejections of claims 1, 9, 15 and 23 are deficient and that these claims are in condition for allowance. Further, since dependent claims 2-3, 5, 7-8 incorporate the limitations of claim 1, dependent claims 10-11 and 13 incorporate the limitations of claim 9, dependent claims 16-17, 19 and 21-22 incorporate the limitations of claim 15, and dependent claims 24, 25 and 27 incorporates the limitations of claim 23, Applicant respectfully assert that these claims also are in condition for allowance.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 

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